Express Mail Label No. EL 935282235 US
Docket No.: S1022. 81244US00
Mailed: May 13, 2005

Amendments to the Written Description of the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

On page 1, after the title insert: --Background Of The Invention--;

On page 1, after "Background of the Invention" but before the first paragraph insert: --1. Field of the Invention--;

On page 1, before the second paragraph beginning on line 10, insert --2. Discussion of the Related Art--;

Please amend the three paragraphs beginning on page 1, line 6 through page 2, line 3, as shown below:

--Fig. 1 schematically shows an integrated circuit 10 comprising a microprocessor (μP) 12, an internal memory (MEM) 14, and input/output terminals (I/O) 16. Microprocessor 12 is intended to execute a program or [[a]] software stored in memory 14. Under control of the program, microprocessor 12 may process data provided by input/output terminals 16 or stored in memory 14 and reading or writing data through input/output terminals 16.

To check the proper operation of the microprocessor, a monitoring circuit 18 is generally integrated ~~to~~ on integrated circuit 10. Monitoring circuit 18 is capable of reading specific data provided by microprocessor 12 on execution of a program, and of possibly performing a processing on the read data. Test terminals 22 connect monitoring circuit 18 to an analysis tool 24. Analysis tool 24 may perform a processing of the received signals, for example, according to commands provided by a user, and ensure a detailed analysis of the operation of microprocessor 12. In particular, analysis tool 24 may determine the program instruction sequence really executed by microprocessor 12.

The number of test terminals 22 for a conventional monitoring circuit 18 may be on the same order of magnitude as the number of input/output terminals 16 of microprocessor 12, for example, from 200 to 400. Test terminals 22 as well as the connections of monitoring circuit 18 take up a significant silicon surface area, which causes an unwanted increase in the circuit cost.

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For this purpose, a first version of integrated circuit 10 comprising monitoring circuit 18 and test terminals 22 is generated in small quantities to adjust the program of microprocessor 12 or "user program". After this adjustment, a version of integrated circuit 10 ~~free of~~ without monitoring circuit 18 and ~~of~~ without test terminals 22 is for sale. This ~~implies the performing of~~ requires providing two versions of the integrated circuit, which requires a significant amount of work and is relatively expensive. Further, the final chip is not necessarily identical to the tested chip.--

Please amend the third full paragraph on page 2, lines 14-18, as shown below:

--Thus, standard IEEE-ISTO-5001, in preparation, provides in its 1999 version, accessible, for example, on website www.ieee-isto.org/Nexus5001, a specific message exchange protocol between a monitoring circuit and an analysis tool for a monitoring circuit 18 requiring but a reduced number of test terminals 22.--

Please amend the first full paragraph on page 3, lines 4-14, as shown below:

--Certain microprocessors can execute in parallel several instructions of the program. For example, a jump instruction can be executed simultaneously with a instruction for reading from and/or writing into memory 14. In such a case, two or three messages are generated at the same time. To store several messages generated at the same time, a solution consists of storing these messages at the same time in a same box of the buffer memory. This compels ~~to increase~~ increasing the storage capacity of each box and thus of increasing the size of the buffer memory. This problem is all the greater as the microprocessor is ~~likely to execute~~ capable of executing a large number of instructions at the same time. Further, according to the standard, an execution of ~~a~~ the same instruction can generate messages of different types.--

On page 3, before line 14, insert --Summary of the Invention--;

Please amend the second full paragraph on page 3, lines 15-19, as shown below:

--An object of the present invention is to provide a monitoring circuit according to standard IEEE-ISTO-5001 which enables monitoring a microprocessor, ~~likely to generate~~ capable of generating a large number of messages at the same time, and having a buffer memory of reduced size.--

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Please amend the two paragraphs beginning on page 3, line 22 through page 4, line 9, as shown below:

--For this purpose, the present invention provides, when several types of messages are likely to be generated at the same time, dividing the buffer memory into several blocks, each of which is provided to only receive messages from ~~on~~ one of the message types likely to be generated at the same time, the size of each block depending on the frequency at which the messages can be stored therein.

More specifically, the present invention provides a monitoring device integrated ~~to~~ on the chip of a microprocessor executing a sequence of instructions, comprising: a message calculation means for generating digital messages of different types each corresponding to the execution of an instruction from among a plurality of predetermined instructions, the calculation means being ~~likely to generate~~ capable of generating several types of messages at the same time; a buffer memory divided into several blocks, each of which is provided to only store messages of one of the types of messages likely to be generated at the same time, the size of each block depending on the maximum frequency at which the messages can be stored therein; and a means for, each time one or several messages are simultaneously stored in blocks of the buffer memory, storing in a predetermined block of the buffer memory a coded value designating said blocks of the buffer memory.--

Please amend the last paragraph on page 5, lines 23-31 as shown below:

--According to an embodiment of the present invention, each message is formed of one or several data, where two messages can be formed of data of the same type and/or of data of different types, and at step b/ each of the data forming the messages generated at step a/ is stored in a sub-block of the buffer memory provided to only store a single type of data, the coded value indicating in which sub-blocks the data have been stored; and

step c/ ~~consists~~ comprises of recovering the coded value written at step b/, and based on said coded value, recovering the data of messages stored at step b/ and restoring the message(s) generated at step a/.--

On page 6, before line 7, insert –Brief Description of the Drawings--;

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On page 6, before line 15, insert --Detailed Description--;

Please amend the three paragraphs beginning on page 6, line 17 through page 7, line 2 as shown below:

~~Same~~ The same reference numerals designate the same elements in the different drawings. Only those elements necessary to the understanding of the present invention have been shown.

Fig. 2 schematically shows an integrated circuit comprising, as in Fig. 1, a microprocessor 12 connected to an internal memory 14, to input/output terminals 16, and to a monitoring circuit 18'. Circuit 18' comprises a calculation circuit 26 receiving information about the instructions executed by the microprocessor, identifying the concerned instruction type and calculating messages provided by the terminal. Calculation circuit 26 is connected to a buffer memory 28 according to the present invention, itself connected to analysis tool 24 via an interface circuit 30 and test terminals forming a parallel access 32.

According to the present invention, buffer memory 28 is divided into several message storage blocks, five in the shown example, A, B, C, D, and E, and an additional block F. An embodiment of the present invention in which calculation circuit 26 is ~~likely to identify~~ capable of identifying five types of events likely to simultaneously or separately occur and to generate messages corresponding to each of these events will be described hereafter.--

Please amend the first full paragraph on page 10, lines 2-8, as shown below:

--The present invention has been described in relation with a specific division of the buffer memory in the case where all types of messages generated by the calculation circuit are likely to be generated at the same time. Those skilled in the art will easily adapt the present invention to the case where each block of the buffer memory can receive various types of messages ~~unlikely to~~ that may not necessarily be generated at the same time.--

Please amend the first two full paragraphs on page 11, lines 4-14 as shown below:

-- The present invention has been described in relation with a calculation circuit 26 ~~likely to~~ capable of simultaneously ~~generate~~ generating five message types, but those skilled in the art will readily adapt the present invention to a calculation circuit likely to generate a greater

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number of messages at the same time. As an example, the calculation circuit may be provided to generate, at the same time, the five message types described in relation with Fig. 2, and a repetition message such as described in application N°PCT/FR02/03526 (B5731PCT), which is incorporated herein by reference.

Further, those skilled in the art will readily adapt the present invention to a microprocessor ~~likely to execute~~ capable of executing, at the same time, two instructions of the same type, such as two read instructions. It provides, for this purpose, a block of the buffer memory for the message corresponding to each instruction.--

On page 11, line 25, please insert:

--Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:--